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A recent study in surface preparation of silicon carbide (SiC)

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Abstract
For any semiconductor material, the fabrication of electronic devices that take the full advantage of the material physical properties requires a perfect control of all technological steps. In an effort to improve silicon carbide (SIC) substrates surfaces prior to epitaxial growth, two chemo mechanical polishing (CMP) techniques were investigated. The results are compared with a mechanical polishing procedure involving various grades of diamond paste. The goal of the present contribution is to recapitulate the important progresses made during past few years in the field of surface preparation of wide band gap materials. We voluntarily focus on our results, which spread out along two main axes. The first is the extension of the Si- face know- how to other types of SiC surfaces and to other wide band gap materials. The second axis concerns the polishing and planarization of epitaxial layers. The industrial implementation of polishing processes and perspectives for future developments is also discussed.
Keywords: - Silicon carbide (SIC), Chemo mechanical polishing (CMP), SiC surfaces.

1. Introduction

In 2004 a detailed review of the state of the art and existing methods of SiC surface preparation has been given. Since then numerous new solutions have been proposed by various research groups. Without being exhaustive, one can mention the improvements of the low removal rate of classic CMP process by means of nonselective CMP (ACMP) or through the introduction of high rate CMP slurries. An innovative planarization approach, replacing the CMP step by catalyst-referred etching (CARE) has been proposed by Okamoto et al. The progressively decreasing feature size of the circuit components has tremendously increased the need for global surface planarization of the various thin film layers that constitute the integrated circuit (IC). Global planarization, being one of the major solutions to meet the demands of the industry, needs to be achieved following the most efficient polishing procedure. Chemical mechanical polishing (CMP) is the planarization method that has been selected by the semiconductor industry today. CMP, an ancient process used for glass polishing, was adopted first as a microelectronic fabrication process by IBM in the 80 s for SiO2 polishing.
For any semiconductor material, the fabrication of electronic devices that take the full advantage of the material physical properties requires a perfect control of all technological steps. The purpose of surface preparation steps – like epi-ready polishing of substrate wafers, planarization of too rough epilayers or reclaim of defective deposits from the substrate – is to provide the best possible surface before further technological stages which inherently deteriorate the surface smoothness. It is well known that in the case of silicon carbide, the high chemical inertia and important hardness of the material make damage free surface preparation a real challenge. Ultimate preparation of SiC surfaces has been for the first time reported at the beginning of that decade. The proposed Step SiC process, based on a combination of mechanical and chemi-mechanical polishing (CMP) produced surfaces free of scratches and subsurface damage on 2-inch, Si-face 4H- and 6H-SiC wafers. The reported RMS surface roughness was respectively <1Å and <1.5Å.
Chemical mechanical polishing (CMP) has emerged as a critical technique for the manufacture of complex integrated circuits to achieve low surface roughness and high degree of planarization. In particular, the continuous progression of the wafer carrier has been driven by the interest of diminishing the waste on a wafer by reducing the edge of exclusion area,

and hence, increasing the amount of chips per wafer. The trend of the new generation materials and devices has driven the continuous demand for super-smooth surfaces and ultra-precision machining quality for silicon carbides (SiC) single crystal wafer. Because chemical mechanical polishing (CMP) is the last process in the ultra-precision machining of SiC single crystal wafer, furthermore, it is also a widely used high-precision global planarization technology. This technology can effectively balance the flatness. Warp and surface roughness (Ra).

In an effort to improve silicon carbide (SIC) substrates surfaces prior to epitaxial growth, two chemo mechanical polishing (CMP) techniques were investigated and the results are compared with a mechanical polishing procedure involving various grades of diamond paste. To achieve efficient planarization at miniaturized device dimensions, there is a need for a better understanding of the physics, chemistry and the complex interplay of tribo-mechanical phenomena occurring at the interface of the pad and wafer in presence of the fluid slurry medium. In spite of the fact that CMP research has grown by leaps and bounds, there are some teething problems associated with CMP process such as delamination, micro scratches, dishing, erosion, corrosion, inefficient post-CMP clean, etc.; research on which is still developing. The fundamental understanding of the CMP is highly necessary to characterize, optimize and model the process. The CMP process is ready to make a positive impact on 30% of the US$ 135 billion global semiconductor market.

Currently, however, its processing parameters mainly rely on production experience for control, which results in poor surface quality and a low machining efficiency. So some researchers have focused on the investigation of parameter matching. Neslen et al.. carried out a test on the 4H-SiC CMP to study the process parameters influencing the material removal rate (MRR), temperature, PH value, pressure, and speed. An et al.. Analyzed the impact of the abrasive on the MRR and Ra of 6H-SiC and observed the surface morphology by AFM. Pan et al. obtained a 6H-SiC wafer with a MRR of 105 nm/h and a Ra of 0.174 nm by a double-sided polishing method. The polishing slurry contains 6 wt% H2O2, 0.6 wt% KOH and 30 wt% silica colloidal. However, these studies just considered parts of the influencing factors with no mathematical model. Studies the CMP process parameters of 2 inch 6H-SiC wafer and it establishes a mathematical model to discuss the function of these parameters on the Ra of SiC single crystal wafer.

This work provides a theoretical basis for the adjustment and optimization of the CMP parameters and intelligent control of the CMP equipment in the actual production process. There are several innovations and modifications such as slurry free approach, low down force polishing, abrasive less and nanoparticle slurry approach, etc. that are being carried out in the CMP process. Process such as reverse electroplating and combination of different planarization process, are also trying to compete with CMP for achievement of effective global and local planarization of the wafer. CMP has evolved into one of the most significant process in circuit fabrication. In the circuit fabrication device isolation plays a significant role in improving the performance of the devices. Device isolation is made possible by shallow trench isolation method, which replaced local oxidation of silicon (LOCOS) in the recent times. STI allows scaling down the device dimensions and more dense packing. CMP of the deposited insulator over the etched transistor active area during STI is necessary. STI is one of the many technological advances in the recent times, which supports shrinkage of the device dimensions. STI provides a good prototype for CMP, which will be carried out for many such advances.

The process of chemical mechanical polishing is also finding increasing application in the field of giant magneto resistive (GMR) and colossal magneto resistive (CMR) disc drives for polishing successive layers of thin films (Co and Ni). Special emphasis is laid on successful endpoint detection and selectivity of the slurry. CMP is used to polish multi-level thin film structure of the drives. The field of micro electromechanical systems (MEMS) is also increasing adapting the process of CMP. For optical MEMS applications the mirror like smooth surface of the thin films is of utmost importance for reliable and repeatable functioning of the device, for example, optical features.

Metal and high-k insulators have replaced the dummy gates, which were used to preserve self alignment of gate electrode. These metal and insulator layers need to be planarized with utmost control, where CMP has to play a significant role. Deposition techniques for such metal and high-k insulator films are yet to be defined and CMP of films deposited by such atomic layer depositions need to be investigated to get optimum polishing performance. Also, CMP of noble metals, which are used to make gate electrodes in p-channel devices need to be investigated to achieve optimum removal performance.

2. Experimental Procedures

2.1 Principle and Process

The CMP technique has the dual behavior of chemical and mechanical action. Its action mechanism is that the revolving wafer is fixed on the polishing carrier and pressed on the flexible polishing pad, which rotates in the same direction. At the same time, polishing slurry can continuously flow between the wafer and the polishing pad. There are the chemical reactions On the wafer surface. The main ionic equation of the Si side of SiC single crystal wafer is as follows.

$$Si + 2OH(-) + H2O \square SiO3(2-) + 2H2$$

The chemical stability of SiC single crystal is very high, but the layer of dangling bonds from Si atoms (Si-face) is unstable. The surface atoms of SiC can easily penetrate into the polishing slurry and react with the alkali to form a water soluble silicate. The abrasive can make it fall off without damaging the SiC single crystal, meanwhile exposing a new surface. This is a cyclic process. Eventually, the ultra precision surfaces form under the combined action of the wafer, abrasive and polishing slurry. A structural schematic of the CMP is shown in Figure.

2.2 Materials and Equipment

The experiment materials of the 2 inch 6H-SiC (0001) wafer are provided by the state key laboratory of crystal materials at Shandong University. The one-side polish test is performed with the precision surface polishing machine named K600SQ, and the SiO2 colloidal is used as the abrasive with an appropriate amount of oxidant (5 wt% H2O2 to make the alkaline (0.8 wt% KOH) polishing slurry. The surface roughness of the SiC single crystal wafer is measured by AFM.

2.3 Experiment Design

Orthogonal test design can make a comprehensive analysis with fewer trials. It not only clarifies the impact of each factor on the test results, but it can also distinguish the primary and secondary factors. This makes it possible to select the optimum level combination. The test uses orthogonal arrays L25 (56) to design an orthogonal test of the six factors and five levels in the following constant conditions: room temperature 250C, and the rotation speed of the polishing carrier nw D60 r/min, which analyses the influence of the process parameters on the MRR and Ra. In the experiment, factor a means the polishing pressure, factor B means the speed of the polishing disk, factor C means the abrasive diameter, factor D means the polishing slurry PH value, factor E means the polishing slurry concentration SiO2, and factor F means the polishing slurry flow. The test factors and design levels are shown in Table 1.

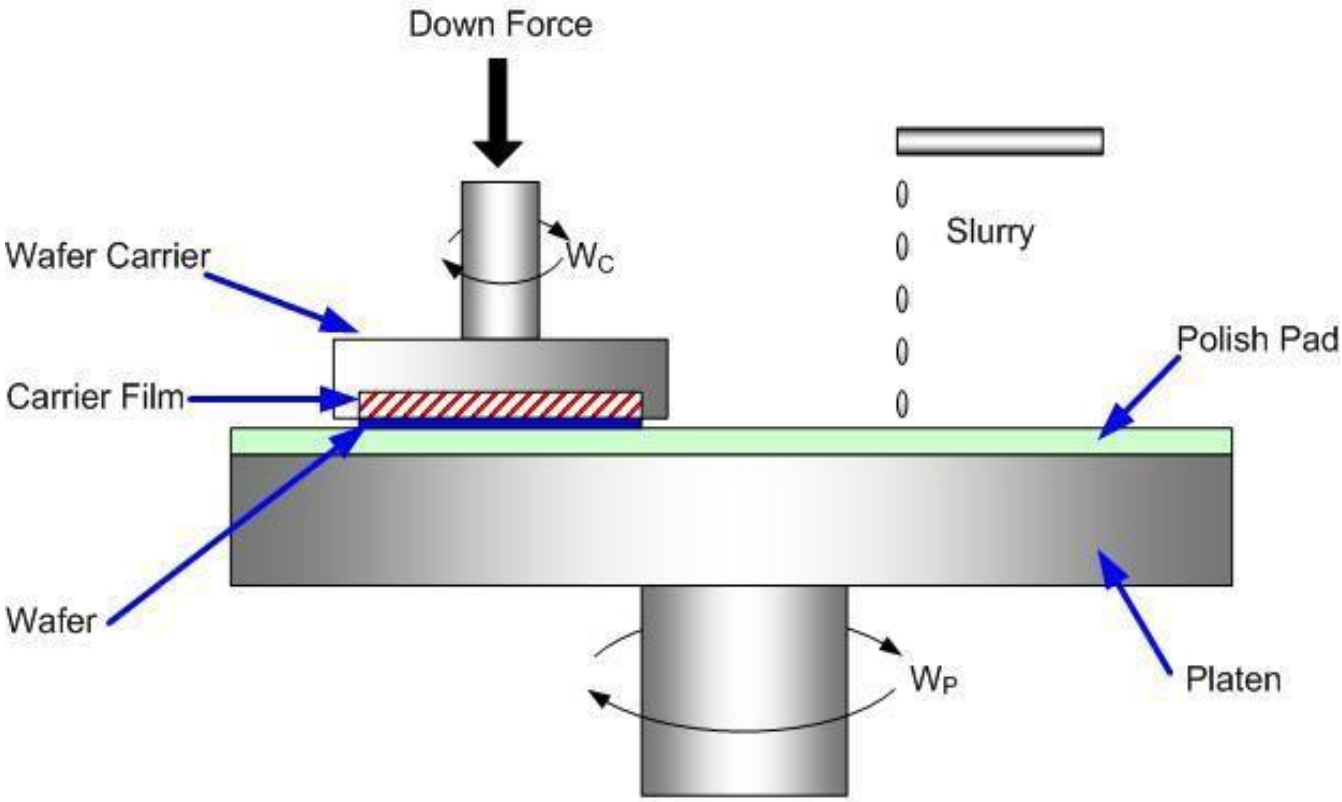

Figure-1 Schematic of a first generation CMP tool

Table-1 Test factors and design levels

Factor	Level				
	1	2	3	4	5
A: p (kPa)	10	11	12	13	14
B: np (r/min)	40	50	60	70	80
C: d (nm)	40	50	60	70	80
D: PH	8	9	10	11	12
E: w (wt%)	5	10	15	20	25
F: q (mL/min)	60	80	100	120	140

3. Results and Discussion

The target of the present contribution is to recapitulate the important progresses made during past few years in the field of surface preparation of wide band gap materials. We voluntarily focus on our proprietary results, which spread out along two main axes. The first is the extension of the Si-face know-how to other types of SiC surfaces and to other wide band gap materials. The second axis concerns the polishing and planarization of epitaxial layers. The industrial implementation of polishing processes and perspectives for future developments will also be discussed.

In order to achieve more visual test results, we use the trend chart. The two CMP techniques utilized (i) chromium oxide(iii) abrasives and (ii) colloidal silica polishing slurry. The best surfaces were obtained after colloidal silica polishing under conditions that combined elevated temperatures (55°C) with a high slurry alkalinity (pH > 10) and a high solute content. Cross-sectional transmission electron microscopy showed no observable subsurface damage, and atomic force microscopy showed a significant reduction in roughness compared to commercial diamond- polished wafers. Growth experiments following colloidal silica polishing yielded a much improved film surface morphology.

A standard wafer carrier and the state of the art Titan™ wafer carrier are compared and evaluated by planarizing a set of blank wafers with a PECVD oxide film on an IPEC 472 CMP tool. The surface roughness was analyzed before and after the planarization step using an atomic force microscope (AFM) and the nonuniformity across the wafer was characterized by ellipsometry. The material removal rate and the reproducibility of the nonuniformity from wafer to wafer was also observed and compared. A second set of experiments with patterned wafers planarized with the Titan™ carrier was also performed. The impact of the pattern density in the step height reduction ratio and surface roughness was analyzed with AFM. The results obtained from the blank wafers planarized with the standard wafer carrier showed a nonuniformity average of ± 6.96% with a 3 mm edge of exclusion, a wafer to wafer nonuniformity of ± 4% and a surface roughness of 0.34 nm. However, the Titan™ carrier delivered a nonuniformity average of ± 2.17%, a wafer to wafer nonuniformity of ± 0.3% and a surface roughness of 0.22 nm. The Titan™ carrier outmatched the standard wafer carrier forcing it to shift the edge of exclusion area to 7mm to be able to achieve a nonuniformity of ± 2.90%. The results for the set of patterned wafers showed a step height reduction ratio (SHRR) average of 98.35%. The surface roughness for the oxide above the patterned polysilicon structures decreased from 9.46 nm to 0.33nm.

We recapitulate the state of the art of silicon carbide and related materials polishing. Since the demonstration of an ultimate preparation of Si-face -SiC wafers some important progresses were made in the field of surface preparation of silicon carbide and related materials. Take the five levels of the six factors as the abscissa and the MRR and Ra as the ordinate. According to the experimental results, when factor A increases in the scope of 10–13 kPa, the MRR significantly improved. Whereas, excess pressure will lead to wafer surface scratches, deformation, etc. Both Ra and sub-surface damage are increased while wafer surface quality decreased. With the relative speed reduction between factor B and the speed of the polishing carrier, the MRR will reduce.

When the relative velocity ratio of polishing disk to polishing carrier is close to 1, this will achieve a good surface quality and the uniformity is also good. Within the scope of the test, the bigger the particle diameter, the higher the MRR is, while factor C has little effect on the Ra. When factor D is around 10, the polishing slurry shows as being weakly alkaline, then the MRR and Ra are both good. With increasing the polishing slurry concentration, the MRR will increase. However, if the concentration is too high, the chemical corrosion will become more serious, causing the wafer surface to have pits. The Ra begins to increase when over a certain concentration; therefore, factor E is appropriate for 20–30 wt%. Besides, if the polishing slurry flow is too small, the polishing slurry supply is inadequate, causing the friction on the wafer surface to rise sharply, which results in a non uniform temperature distribution and instability. Conversely, the excessive polishing slurry flow will cause use insufficiency, which increases the cost of polishing. Consequently, it requires us to adjust factor F appropriately. Among all these factors, A and B reflect the mechanical action while C, D, E and F reflect the chemical effect. As the particularity of the CMP process, in order to achieve optimal results, we need to balance the mechanical and chemical action. Therefore, the key is to coordinate and control the CMP process parameters.

4. Modeling

The results of the orthogonal test show that the three most important factors which impact the Ra of the wafer are the polishing pressure, polishing slurry concentration, and the relative velocity ratio of polishing disk to polishing carrier. To establish a more accurate model for CMP, we improve the test and design the three factors and three levels of quadratic orthogonal regression test.

Table-2 Verification of test results

No.	x_1	x_2	x_3	Y(Measure)	Y(Calculate)	Relative Error
2	14	30	0.9	0.47	0.4489	0.0448
10	8.6	20	1.2	0.5	0.4808	0.0385
14	12	20	0.6	0.41	0.4131	0.0076
add1	11	25	1.1	0.36	0.3468	0.0367
add2	9	28	0.9	0.47	0.4622	0.0167
add3	13	14	1.0	0.41	0.3922	0.0435

5. Conclusions

The paper begins by stressing the importance of research in the STI and BEOL processes. It discusses the need for planarization and different techniques of planarization. It can be seen from the 208 P.B. Zantye et al. / Materials Science and Engineering discussion that the technique of chemical mechanical polishing offers tremendous benefits over the other available techniques at present. The technique of CMP is especially suitable for shallow trench isolation of devices and fabricating dual damascene structures for interconnects. The research paper tries to understand the exact science of the CMP process. The mechanism of material removal and planarization strictly depends upon the material that is being removed. The CMP process has different material removal mechanism and surface tribochemical interaction for silicon di oxide, polymers, metals and ceramics. The different efforts for the theoretical characterizations of different surface interactions have been mentioned in the paper. That gives a brief outline of the physical process of CMP and industrial standards that are followed while performing different CMP processes at different times during the semiconductor device fabrication.

The dependence of the CMP process, its surface chemical reaction, abrasive wear and the associated output parameters such as removal rate, global planarization, uniformity, surface roughness, etc. on the input variables such as spindle speed, down force, slurry flow and platen rotation has been discussed at length. Consumables form an important part of the overall CMP process. This paper presents a review of the various pads, different types of slurries, retaining rings and other consumables available in the market and under research at this time. The consumable parameters such as pad porosity, hardness, elasticity, slurry pH, slurry chemistry and its effect on the CMP process parameters such as removal rate and process defects have been reviewed. The paper goes in details of the different CMP process employed to polish dielectrics, metals and ceramics. The various issues that arise during the polishing of various doped and undoped oxide, soft and inherently weak polymeric materials used as dielectrics, novel aerogels and xerogels presently under consideration for implementation as future dielectrics have been discussed at length. It also dwells on the CMP of tungsten plugs, Cu and Al interconnects, as well as Pt CMP for some specialized application. The post-CMP issues such as particle adhesion, corrosion and surface scratches have also been discussed. Due to the implementation of novel thin films in the integrated circuits, the issues such as weak interfacial adhesion are influence the CMP of these materials a lot. The weak interface gives rise to a catastrophic failure of the polishing thin film known as delamination.

The material that is being polished also can have a lot of micro scratches as at the end of a CMP process. Due to agglomeration of smaller particles in the slurry, a large chunk of particulate materials comes in contact with the slurry there by causing the microscratches to occur on the surface. Dishing reduces the final thickness of copper lines and degrades the planarity of the wafer's surface, resulting in complications when adding multiple levels of metal. By definition, it is the difference in the SiO2 thickness before and after polishing. The pattern density dependant defects of dishing and erosion are also vigorously being studied by the semiconductor industry today. The process optimization issues such as lowering the within and across-wafer polish rate non-uniformities to achieve the required statistical process control metrics and effective process end point detection have been discussed. The process defects in CMP occur not only during the actual polishing but also during the post- CMP clean operations. Defects like metal corrosion occur as the wafer is cleaned in highly voracious post-CMP clean environments. The paper talks in brief on the various post-CMP clean mechanisms presently being employed and the ongoing efforts to minimize the defects that occur on the wafer during the post-CMP clean process. Post-CMP metrology is very important to determine the accuracy and reliability of the CMP process. The integrity of the surface and pattern has to be accurately determined and evaluated. This paper also presents and overview of the various metrology techniques that have been implemented to evaluate the CMP process and polishing behavior of the various CMP consumables.

We also studied the impact of the CMP process parameters on the MRR and Ra by designing an orthogonal test of six factors and five levels. Among all of the various factors, the impact order rank of the Ra is: the polishing pressure > the polishing slurry concentration > the relative velocity ratio of polishing disk to polishing carrier > the polishing slurry PH value > the polishing slurry flow > the abrasive diameter. Meanwhile, it has also determined that the optimal parameters are the polishing pressure p D12 kPa, the polishing slurry concentration w D 20 wt%, the speed of the polishing disk np D 70 r/min, the speed of the polishing carrier nw D 60 r/min, the polishing slurry PH D 10, the polishing slurry flow q D 120 mL/min, and the abrasive diameter d D 50 nm. Finally, it has preformed the verification and application of the regression equation model. It is concluded that the model can predict well the test results to a certain degree.

Conflict of Interest

In this manuscript the authors declare that there is no conflict of interest.

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