ISSN: 2455-1848
International Journal of Innovative Research & Growth
A Peer Reviewed & Referred International Journal
Volume-4 Issue-4 February-2017
Impact Factor-2.58
www.ijirg.com, editor@ijirg.com

Analysis Of A Boost DC-DC Converter With Large Conversion Ratio

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Abstract
Large voltage step-up can be achieved without high duty-cycle, with low voltage and current stress and without transformer by introducing A new PWM dc-dc converter. This circuit is Incorporated an extension of the boost interleaved converter, having a multistage capacitor multiplier. For reducing the reverse recovery current of the diodes and also obtaining low turn-on and turn-off losses A simple non dissipative snubber can be used. The flexibility of the structure allows the increment of the current, voltage and power levels, using the same range of components and maintaining high efficiency, by augmentation of the number of series and parallel stages. This paper provides a theoretical investigation, and experimental examined data on a 400W example that was made and tested: 24 Vdc input, 200 Vdc output, and 40-kHz switching frequency. The theoretical predictions and the measured efficiency obtained is measured and agreed well with the equal to 95% at full load.
Keywords: *PWM, Snubber, dc-dc converter.*

1- INTRODUCTION

The step-up power conversion is continuously increasing its applications and power capability demands. Some examples are electric vehicles, unintenupted power supplies *(U P S)* and photovoltaic systems. The he1 cell power system, which is recently gaining a lot of attention as a new alternative power source, presents a low output DC voltage, requiring the use of step-up converters with high static gain.

The boost converter is one of the most important nonisolated step-up converter, however the operation with high input current and high output voltage, became impracticable the development of high performance impracticable the development of high performance. converter, due to efficiency degradation and dynamic range limitation.

Other alternative is the utilization of an isolated dc-dc converters, as the current-fed push-pull converter and the dual inductor-fed push-pull converter [1,2]. The transformer commonly provides two functions in a dc-dc switching converter: it provides dc isolation and an additional voltage conversion ratio over and above that available from the switch duty-cycle. In applications where dc isolation is not necessary, a transformer would normally still be required for large voltage conversion ratio However leakage inductance of the transformer causes some problems as switch voltage overshoot, EMI generation and energy dissipation in snubbers [3]. Therefore, the high input current associated with the non-idealities of the circuit operating with hard-switching, reduce the converter efficiency.

Recently, the active clamping technique was used in the current-fed isolated converters, operating with soft commutation [4,5]. However, this alternative presents as drawback a high switch voltage stress.

In order to overcome the limitations of the classical topologies for high-power and large conversion ratio applications. a new non isolated structure is proposed in this paper. The main advantages of the proposed structure are presented below. High static gain is obtained with the use of a multiplier stage integrated to the structure.The current stress in all components are reduced by the use of the

interleaved technique. Low input current and output voltage ripple are obtained due to the interleaved operation. Low voltage and current stress in the power switches, resulting in low conduction losses. **0** Reduction of the turn-on and turn-off losses including a simple non dissipative snubber. High efficiency in high power applications due **to** the reduction of the conduction and commutation losses and with the elimination of the power transformer. The modularity of the structure allows the increment of the current, voltage and power levels. using the same range of components and maintaining high efficiency, only increasing the number of series and parallel stages. The features of the proposed converter are discussed in this paper and the principle of operation, design procedure, simulation and experimental results are presented to validate the solution proposed.

2- PROPOSED STRUCTURE

A. Circuit Description

A generic configuration of the proposed structure is shown in Fig. 1. This converter is based on the interleaved boost converter, integrated with multiplier capacitors connected in series. These capacitors present a comportment similar to the series capacitor of the Sepic converter, however these capacitors allow to obtain high static gain. The number of parallel stages is represented by the parameter **"P"** and the number of multiplier stages is represented by the parameter "M", that are defined by the number of the multiplier capacitors (C,) in series with each switch. In order to simplify the description and the explanation of the principle of operation of the proposed converter, will be considered the minimum configuration, that is composed by two stages in parallel (P=2) and one series multiplier stage (M=l), as shown in Fig **2.** The theoretical analysis developed for the minimum configuration can be extended for the generalized structure, considering its modularity. The number of stages in series and parallel will be defined by the relation between the output and input voltage and by the maximum switch voltage and current stress. As the proposed structure is derived from the boost converter, there is one input inductor **(L1** and L2) for each stage connected in parallel. The design of his inductor is the same of the classical boost converter.

The input current ripple is reduced by the number of parallel stages operating with different phases. The capacitors C_{m1} and C_{m2} and diodes D_{Mi} and D_{M2} are the main difference of the proposed structure in relation to the boost interleaved converter. These capacitors will be charged by the diodes D_{M1} and D_M, with a voltage V_M that is equal to the output voltage of the classical boost and is equal to the voltage across the power switches. However, due to the configuration of the circuit, the output voltage is equal to (M+l) times the voltage V_M ,but the maximum switch voltage will be always equal to VM. This characteristic allows to eliminate the power transformer in high static gain applications, without the increment of the switch voltage. The diodes Ds_2 and D_{S2} are the output diodes and operate like the output diodes of the interleaved boost converter. The output filter and load are represented by C_O and R_O.

B. Principle of Operation

The principle of operation is presented considering ideal components. The proposed structure presents different stages operating in continuous and discontinuous conduction mode and with a duty-cycle (D) lower and higher than 0.5. The operation in continuous conduction mode and D>0.5 is presented below. The main theoretical waveforms considering ideal components and D>0.5are shown in Fig. 3.

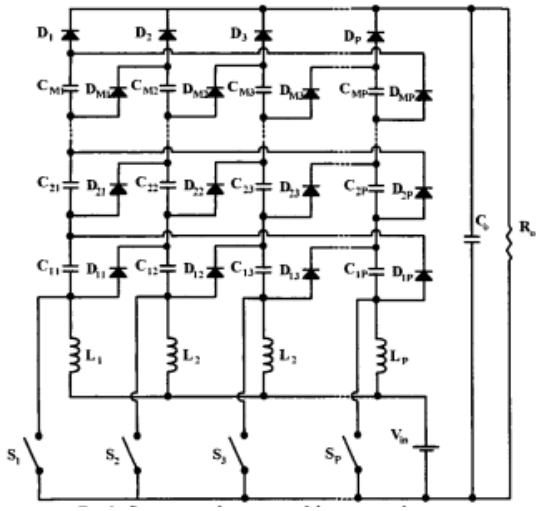

Fig.1 Generic configiirtion of the proposed converter.

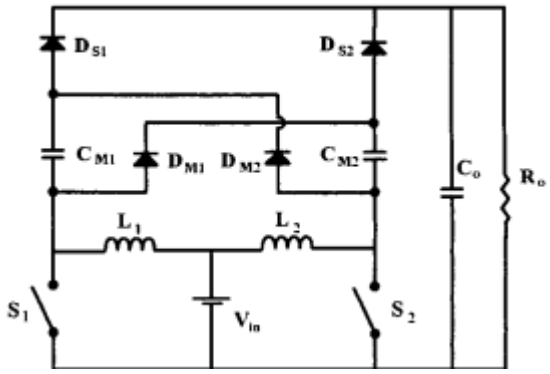

Fig. 2 Minimal configuration of the proposed converter (P=2,M=1)

1) First Stage ([to, t J Fig. 4).
Both switches are conducting and the inp ut current flows through the input inductors and power switches. All diodes are blocked and the input inductors store energy during this stage

2) Second Stage ([t_1,t_2] Fig. 5)
At the instant tl, switch S2is turned-off and the energy stored in the input inductor L2 is transferred to the output capacitor C_o through the diode D_{s2} and also to the multiplier capacitor C_{M1} through the diode Dm.
It can be observed in Fig. 5 that the multiplier capacitors CMland *Cm* are connected in series by the diode Dm and connected in parallel with the output capacitor C_O by the output diode Ds_2.Thus. the output voltage will be equal two times the multiplier capacitor voltage (VO=~.VM) and equal to ($Vo=V_M.(M+l)$) **for** the generic structure. The maximum voltage applied across the switch S_2 is equal to the C_{M1} capacitor \.oltage (VM)and the maximum voltage across the output diode Ds_1 is equal to the *Cm* multiplier capacitor voltage (v h ,) . However, the maximum voltage applied across the multiplier diode D_{M1} is always equal two times the multiplier capacitor voltage ($V_{CM1}+V_{CM2}$).

3) Third Stage ([t.. I;] Fig. 6).
The switch **S2** is turned-on and the input inductors **L1** and Lz store energy as in the first operation stage.

4) Fourth Stage ([t;, I,] Fig. **7) .**
At the instant t,. suitcl1 SI is turned-off and the energy stored in the input inductor I-, is transferred to the output capacitor **CO** and also to the multiplier capacitor Cm_2. As the multiplier capacitor CMl was charged in the second operation stage. The output diode Dsl will conduct first and will present a peak current higher than the multiplier diode Db,,. but both diodes presents the same average current. The diodes average current are reduced by the number of series and pardlel stages. There is an important difference between the classical low frequency voltage multiplier rectifiers and the voltage multiplier integrated with the boost converter proposed in this paper. The increment of the multiplier stages in the classical voltage multiplier. increase the number of diodes connected in series and also increase the conduction losses. Thus, normally there is a reduction of the efficiency with the increment **of** the multiplier stages. However, this not occurs in the proposed multiplier because the current is divided among the various multiplier diodes, as a parallel connection. Therefore, the increment of the multiplier stages does not increase the conduction losses of the diodes.

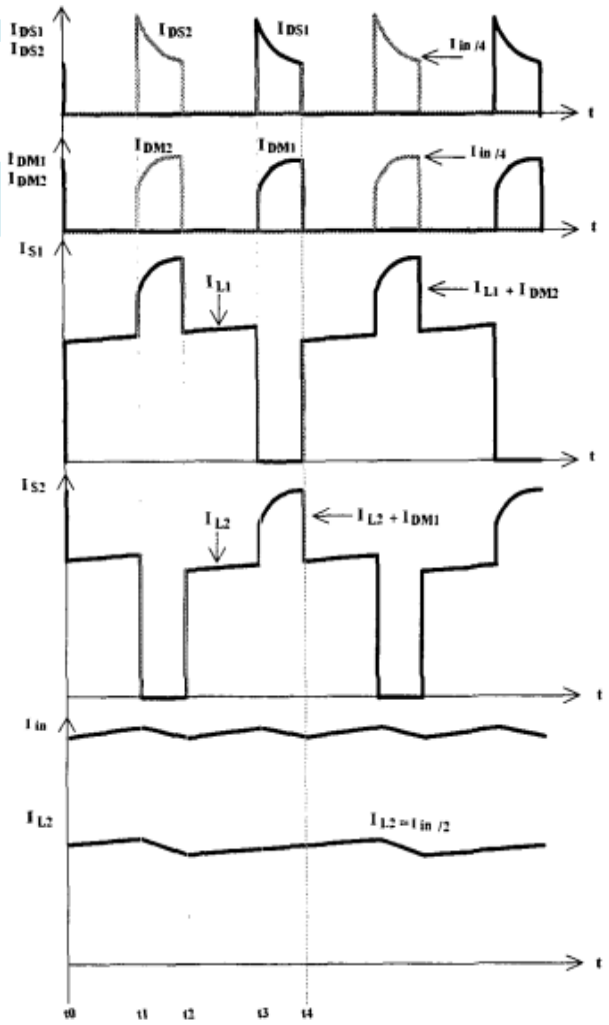

Fig. 3. Main theoretical waveforms(D>0.5)

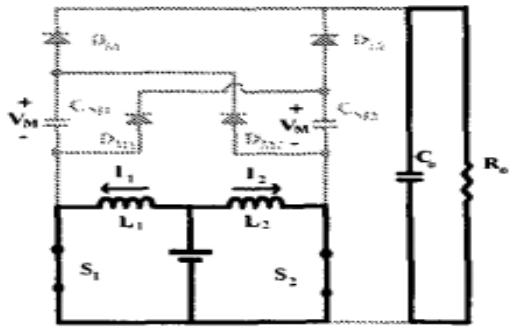

Fig. 4. **First stirge (lo. t,).**

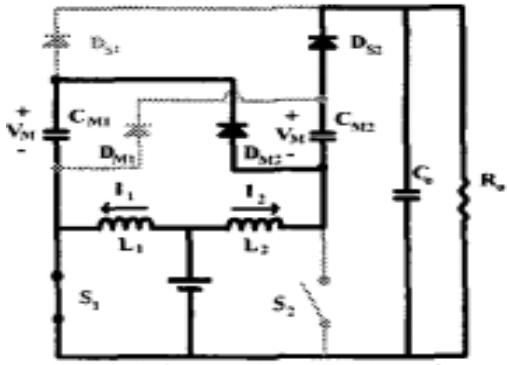

Fig. 5. Second stage (t_1, t_2).

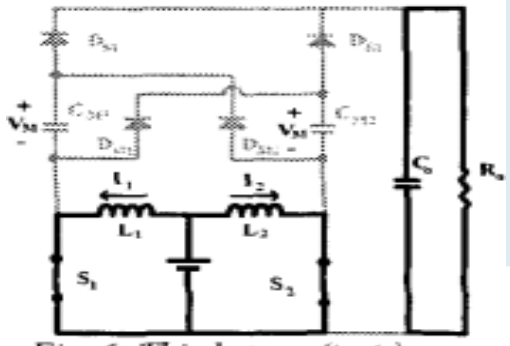

Fig. 6. Third stage (t_2, t_3).

The operation in continuous conduction mode and DL0.5 is presented in Figs 8, **9,** and 10. **As** the proposed structure is developed to operate with high static gain, the theoretical waveforms operating with Dc0.5 are not presented.

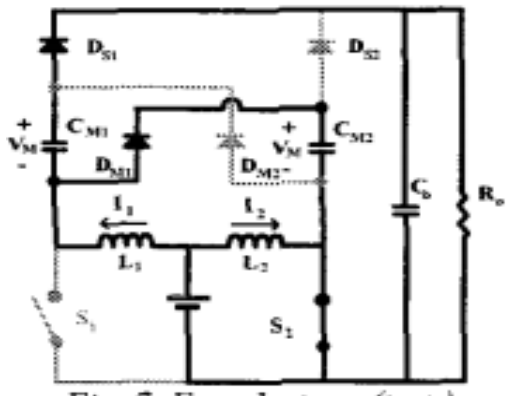

Fig. 7. Fourth stage (t_3, t_4).

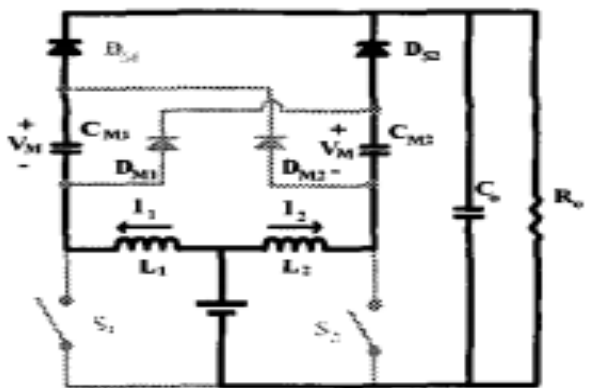

Fig. 8. First stage (DCO.5)

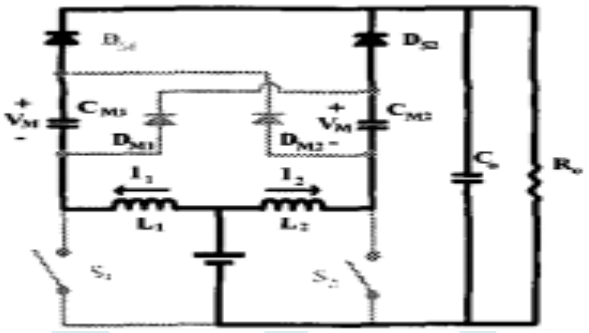

Fig 9 Second stage (D<O5)

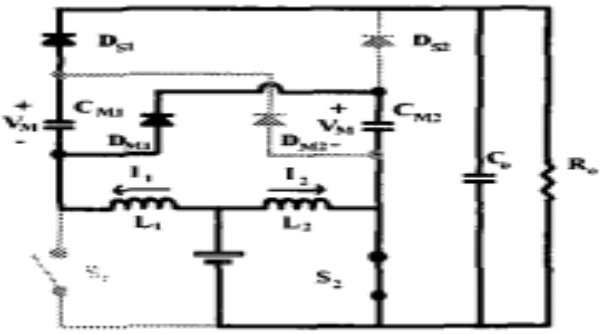

Fig. 10. **Third stuge** (D<0.5) .

Operation stages considering the switch duty-cycle lower than 0.5.

1) First Stage (Fig. 8).

Only the switch $\mathbf{S_I}$ is conducting and the inductor $\mathbf{L_1}$ stores energy. The energy stored in the inductor Lz is transferred to the output through the diode $\mathbf{D_{S2}}$ and the multiplier capacitor C_{M1} is also charged through the diode D_M.

2) Second Stage (Fig. 9)

Switch $\mathbf{S_I}$ is turned-off and the energy stored in the input inductor L_1 is transferred to the output capacitor CO through the diode Dsl. The diode Dsz remains conducting the Lz current. During this stage all switches are turned-off and all multiplier diodes are blocked.

3) Third Stage (Fig. 10).

Switch S_2 is turned-on and the inductor L_2 stores energy. The diode D_{Ml} conducts and charges the multiplier capacitor C_M.

3- MAIN MATHEMATICAL ANALYSISRESULTS

The analysis was realized considering the operation with duty-cycle higher than **0.5.** The main equations obtained in the theoretical analysis are presented with 'a simplified design procedure of an experimental prototype. The specifications considered for implementation and test of the proposed converter are:

Input voltage: V,, = 24V
Output voltage: V, =200V
Output power: Po= 400W
Switching frequency: f = 40kHz
Multiplier stages: M=l
Parallel stages: P=2

A. Staticgain Headings,

The staticgain **of** the proposed converter operating in continuous conduction mode is presented in (1). This equation is also valid for the operation with D<0.5.

$$q = \frac{V_O}{V_O} = \frac{M+1}{1-D} = \frac{200}{24} = 8.333 \quad (1)$$

Where: M- Number of multiplier stages

D-Switch duty-cycle

Thus, nominal duty-cycle is calculated

$$D = V_O - \frac{(M+1)V_{in}}{Vo} = \frac{200-(2.24)}{200} = .76 \quad (2)$$

B. Voltage Stress

The maximum voltage applied across the power switches **(S_I** and Sz)and the output diodes (Dsland Dsz)are equal to the multiplier capacitor voltage **(V,).** The maximum voltage in this components is:

$$V_M = V_S = V_{DS} = V_{in}\frac{1}{1-D} = 24\frac{1}{1-.76} = 100v \quad (3)$$

$$V_{DM} = V_{IN}\frac{2}{1-D} = 24\frac{2}{1-D} = 200 \quad (4)$$

C. Current Stress

The current in all components are divided by the number of parallel stages **(P).** Considering efficiency equal to **94%** operating with nominal output power, the converter input current is equal to:

$$I_{in} = \frac{Po}{V_{in}-\eta} = \frac{400}{24.095} = 17.54A \quad (5)$$

The RMS switch current is calculated by **(6)** considering
the operation with D>0.5.

$$I_{S_{RMS}} = \frac{I_{in}}{P}.\frac{5-D}{4} = \frac{17.54}{2}.\sqrt{1.76} = 9A \text{ N} \quad (6)$$

The average current in each diode is reduced by the number of parallel **(P)** and series stages **(M).**

$$I_{DMAVO} = I_{DSAVG} = \frac{I_{in}}{P.(M+1)} = .(1-D) = \frac{17.54}{2(1+1)} = . \quad (7)$$

$$(1-.76) = 1.05A$$

As can be seen in **(7),** the diode average current is reduced with the increment of the parallel stages **(P)** and with the number of multiplier stages (M). Therefore, the increment of the number of the diodes does not increase the diode conduction losses because the average current of each diode is reduced proportionally.

D. Pussive components

The design of the input inductance is the same of the classical boost converter.

$$L_1 = L_2 = \frac{V_{in}D}{p.\Delta I_l f} = \frac{24.0.76}{2.(17.54.0.125).40.10^3} = 100\mu H \quad (8)$$

z=-Input current ripple

The multiplier capacitor can be calculated by **(9),** where **AVc** is the capacitor voltage ripple.

$$C_1 = C_2 = \frac{I_{in}(1-D)}{P(M+1)\Delta V_c F} = \frac{17.54(1-.76)}{2.2.10.40.10^3} = 2.6\mu F \quad (9)$$

E. Theoretical EfJicienq

The turn-on and **turn-off**losses are minimized by the utilization of a non dissipative snubber. Therefore these losses will not be considered.

The conduction losses of the power switch is calculated by (10). Considering the utilization of the MOSFE 20M22LVR with a drain-source resistance equal to 396mR, operating at 100°C.

$$P_S = \left(I_{S_{RMS}}\right)^2.R_{DS_{on}} = 9^2 \cdot 0.396 = 3.2W \quad (10)$$

The conduction losses of the output diodes and the multiplier diodes are calculated by **(l l) ,** considering a forward voltage **(V,)**

equal to 1.5V.

$$P_D = I_{Davg}.V_f = 1.05*1.5 = 1.575 \quad (11)$$

The magnetic losses of the input inductors are reduced and will not be considered in the efficiency estimation. The conduction losses of the input inductors is calculated by **(12),** where:

R24,, - Area of conductor **(24** AWG)

N -Number of turns

Ncond-Number of parallel conductors

It - Average length of tum

$$P_L = \frac{I_{in}}{2}\frac{R24_{AWG}}{N_{cond}}.It.n.1.3 = (\frac{17.54}{2})2.\frac{.00204}{10}.11.6.10. \quad (12)$$

The efficiency estimation is calculated by:

$$\eta = \frac{P_o}{Po + 2.P_s + 4P_d + 2P_l}.100 \quad (13)$$

Therefore:

$$\eta = \frac{400}{400 + 2.3.2 + 4.1.57 + 2.24}.100 = 95.8\% \quad (14)$$

4- EXPERIMENTAL RESULTS

The practical aspects of the proposed converter and the design procedure developed are verified with the implementation of a laboratory prototype, considering the specifications presented. The power circuit of the prototype is shown in Fig. **1 1 .** A non dissipative snubber was added reducing the reverse recovery current of the diode and also obtaining low turn-on and turn-off losses. Only snubber is necessary for each switch even for various multiplier stage, because the reverse recovery current of all diodes are in series with the snubber inductance.

Fig. 12 present a very important characteristic of the proposed converter that is the reduction of the voltage is equal to 200v and the maximum voltage across the switch is about 120v.

Fig. 13 show the voltage across the output diode(Ds1) . The diode voltage is also reduced.

Fig. 14 shows the turn-on commutation of the switch S_1. The turn-on and turn-off losses are reduced due to the presence of the non dissipative snubber.

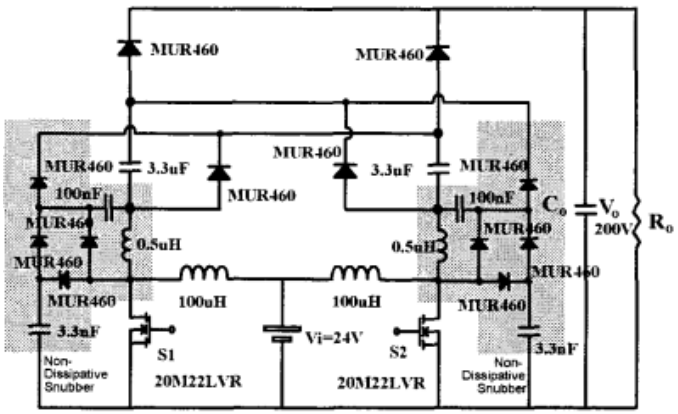

Fig. 11. Power circuit implemented.

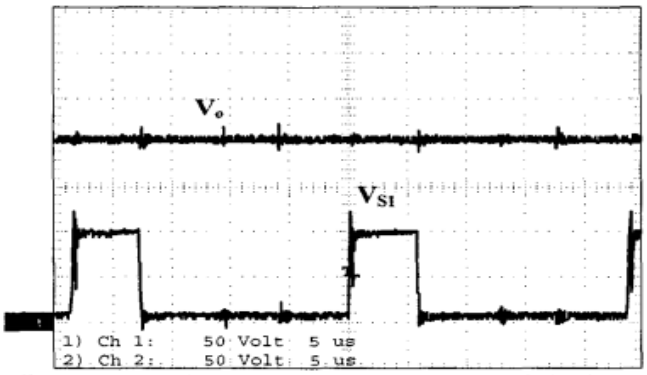

Fig. 12. Output voltage and the power switch voltage (50V/5µs/div).

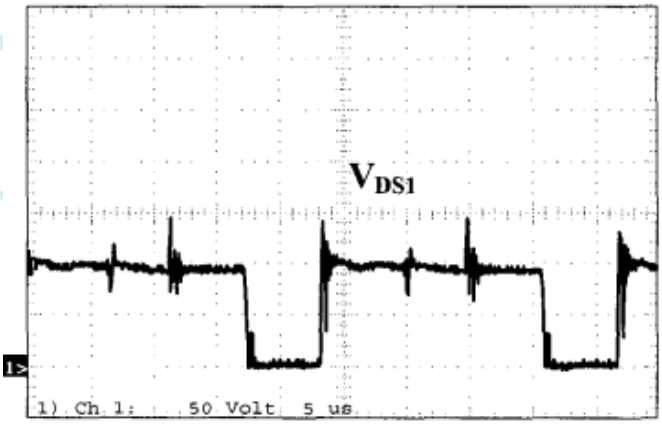

Fig.13- Output diode voltage (50V/5µs/div).

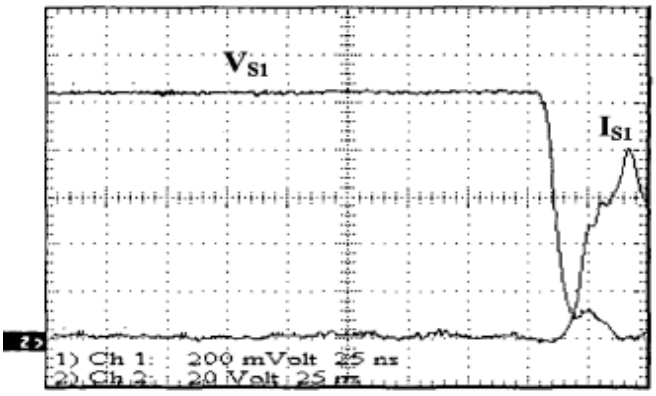

Fig. 14. Switch turn-on commutation (20V/5µs/div).

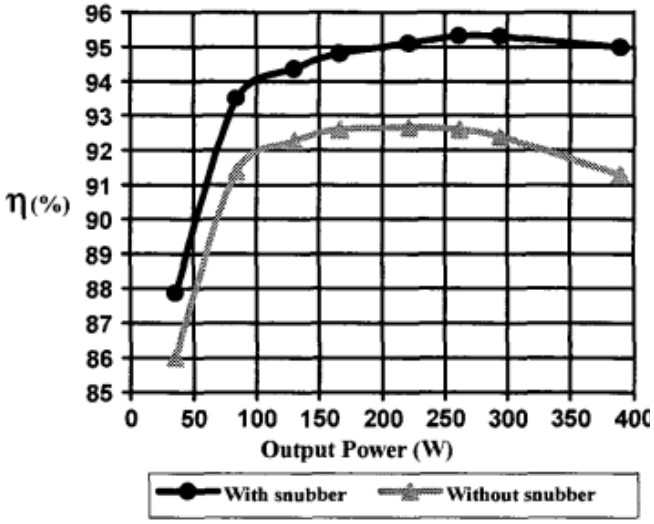

Fig. 15. Measured efficiency of the proposed converter.

The efficiency curve of the power circuit, as a function of the output power. is presented in Fig.15. Considering the use of the non dissipative snubber, the efficiency reached at the nominal load **is** equal **to** *95%*. The utilization of the non dissipative snubber is very important in this structure, because the reverse recovery current of the output diode and multiplier diodes are added. increasing its negative effects as high switch peak current and increment of the turn-on commutation losses. As can be observed in Fig 15, the efficiency reduction is about **4%** in the operation with nominal load, without the non dissipative snubber. It was observed by simulation and in the practical implementation that the current and voltage sharing in the switches and diodes are dependent only of the symmetry **of** the switch duty-cycle. Asymmetries **of** intrinsic parameters of the circuit as inductance. does not change the current or voltage sharing.

5- CONCLUSIONS

The proposed structure allows to operate with large step-up conversions ratio, without a transformer and also maintain low voltage and current stress in the switches and diodes. The operation with high switching frequency and reduced coinmutation losses is possible using a simple non dissipative snubber. The proposed converter presents high efficiency (95%) due to low voltage and current stress and low commutation losses. The modularity of the structure allows the increment of the current, voltage and power levels, using the same range of components and maintaining high efficiency, only increasing the number of series and parallel stages. The experimental results c o n f m the basic operation of the converter and theoretical analysis developed .

6- REFERENCES

The template will number citations consecutively within brackets [1]. The sentence punctuation follows the bracket [2].

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